(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

Appl. No. 09/844,296
Doc. Ref. AF1

(11) EP 1 006 697 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
07.06.2000 Bulletin 2000/23

(51) Int Cl.[7]: **H04L 25/03**

(21) Application number: **99309305.3**

(22) Date of filing: **23.11.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **02.12.1998 US 203969**

(71) Applicant: **LUCENT TECHNOLOGIES INC.**
Murray Hill, New Jersey 07974-0636 (US)

(72) Inventors:
- **Azadet, Kameran**
  Middletown, New Jersey 07748 (US)
- **Yu, Meng-Lin My**
  Morganville, New Jersey 07751 (US)

(74) Representative:
Watts, Christopher Malcolm Kelway, Dr. et al
Lucent Technologies (UK) Ltd,
5 Mornington Road
Woodford Green Essex, IG8 0TU (GB)

(54) Parellel signal processing for equalisation on fibre channels

(57) A method and apparatus are disclosed for reducing dispersion problems in data signals received over a channel, such as a fiber channel. A receiver processes the received data on parallel branches at a rate that is slower than the original clock rate. Channel equalization techniques can thus be applied to fiber channels despite the very high clock rates of the received signal. The clock rate of the received signal is reduced by an arbitrary factor N for sampling and digitizing the analog signal at the output of the fiber channel. The parallel analog samples are digitized before digital signal processing (DSP) techniques are applied by an adaptive digital signal processor to perform data detection. The adaptive digital signal processor may be embodied, for example, as an adaptive channel equalizer that utilizes an adaptive feed forward equalizer (FFE), or as a maximum likelihood sequence estimator (MLSE), such as a Viterbi detector.

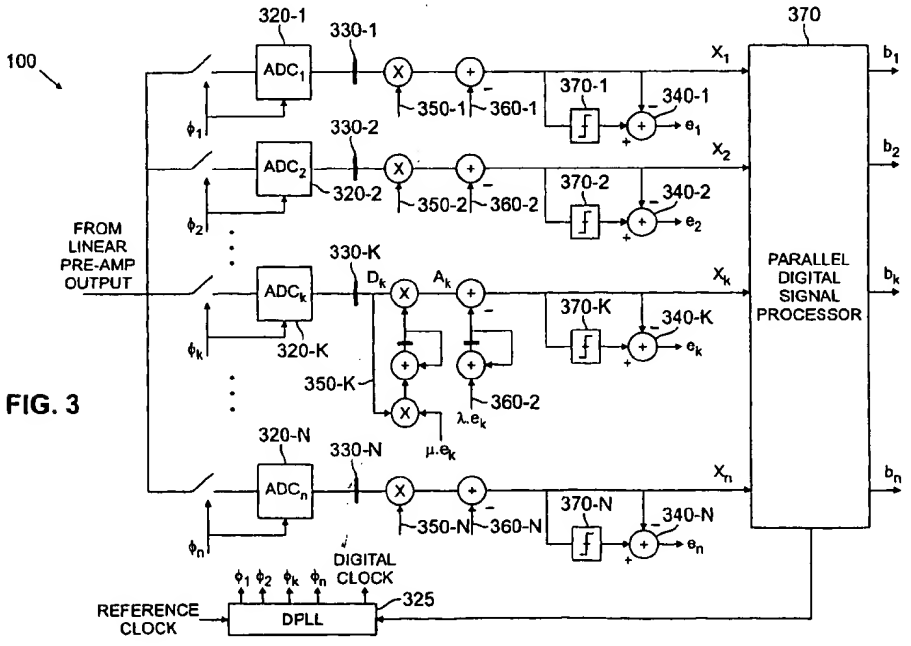

FIG. 3

EP 1 006 697 A2

Description

Field of the Invention

[0001] The present invention relates generally to channel equalization techniques, and more particularly, to channel equalization techniques for reducing dispersion problems in fiber channels.

Background of the Invention

[0002] The transmission rates for local area networks (LANs) have progressively increased from 10 Megabits-per-second (Mbps) using twisted pair conductors to 1 Gigabit-per-second (Gbps) using multi-mode fiber channels. In a multi-mode fiber, the light rays follow different paths, often with their own respective lengths and therefore exhibit delay spread. A result of delay spread in a multi-mode fiber channel is that it considerably reduces the distance over which digital data can be accurately transmitted. Typical fibers used for gigabit transmission have a cutoff frequency specification of 200 Megahertz kilometer (MHz-km). Thus, there is a trade-off between channel lengths and bandwidth. As an example, for a multi-mode 200 Megahertz kilometer (MHz-km) fiber having a bandwidth of 1 Gigahertz (GHz), the cable length should be limited to approximately 200 meters. The Gigabit Ethernet standard, for example, operates at a bit rate of 1.25 Gigabits-per-second (GBps), has a corresponding bandwidth of 612.5 MHz and thus has a maximum channel length of 326.5 meters. In order to guarantee reliable data transmission over all grades and brands of previously installed multi-mode fibers, however, the Gigabit Ethernet standard limits the maximum channel length to 275 meters,. It is desirable, however, to transmit digital signals on a fiber channel over distances of one kilometer or more.

[0003] Although fiber channel lengths for high speed digital signals could be increased by implementing channel equalization techniques in the receiver, such as those channel equalization techniques applied to more non-fiber based channels, e.g., twisted pair conductors, typical fiber receivers have not implemented any kind of sophisticated channel equalization. This is because of the practical difficulty of implementing a channel equalizer that operates at such high clock rates, e.g., on the order of one Gigahertz.

Summary of the Invention

[0004] Generally, a method and apparatus are disclosed for reducing delay spread problems in data signals received over a channel, such as a fiber channel, by processing the received data on parallel branches at a rate that is slower than the original clock rate. The present invention makes channel equalization possible, despite the very high clock rates of the received signal. The original clock rate of the received signal is reduced by an arbitrary factor, N. The received signal is sampled and digitized using N parallel paths that are each triggered with a clock that is 1/N-times as fast as the original clock rate. The converted samples are processed using digital signal processing (DSP) techniques.

[0005] In one implementation, the incoming signal is sampled and digitized in parallel at a clock rate that is 1/N-times as fast as the incoming clock rate. The analog samples are digitized in parallel before digital signal processing (DSP) techniques are applied by an adaptive digital signal processor to perform data detection. The adaptive digital signal processor may be embodied, for example, as an adaptive channel equalizer that utilizes an adaptive feed forward equalizer (FFE), as a combined adaptive feed forward equalizer (FFE) with a decision feedback equalizer (DFE), or as a maximum likelihood sequence estimator (MLSE), such as a Viterbi detector, combined with channel estimation.

Brief Description of the Drawings

[0006]

FIG. 1 is a schematic block diagram of a receiver in accordance with the present invention that reduces dispersion problems in data signals received over a fiber channel;

FIG. 2 illustrates the incoming clock, clk, associated with the received data, and the various 1/N-times slower clocks, Φ_1 through Φ_N, of FIG. 1;

FIG. 3 illustrates one suitable implementation of circuitry for the receiver of FIG. 1 in accordance with the present invention;

FIG. 4 illustrates an adaptive channel equalizer implementation of the receiver of FIG. 1;

FIG. 5 illustrates an implementation of the adaptive channel equalizer of FIG. 4;

FIG. 6 illustrates a maximum likelihood sequence estimation implementation of the receiver of FIG. 1;

FIG. 7 illustrates a schematic block diagram of a parallel channel equalizer, and

FIG. 8 illustrates a parallel finite impulse response (FIR) filter implementation of Equation 6.

Detailed Description

[0007] FIG. 1 illustrates a receiver 100 in accordance with the present invention that reduces dispersion problems in data signals received over a fiber channel 110. According to a feature of the present invention, the receiver 100 processes different portions of the received data on parallel branches at a rate that is slower than the original clock rate. Thus, the present invention makes channel equalization possible for fiber channels despite the very high clock rates of the received signal and appears to perform channel equalization at the original clock rate. As discussed further below, N trigger clocks, Φ_1 through Φ_N, are generated from the clock rate of the received signal. Thus, the clock rate of each of the trigger clocks, Φ_1 through Φ_N, is reduced by an arbitrary factor N for sampling and digitizing the analog signal at the output of the fiber channel 110, and then processing the converted samples using digital signal processing (DSP) techniques. For example, if the bit rate is 1.25 Gigabits-per-second (Gbps), and the receiver 100 includes N=10 parallel processing paths, the signals can be sampled, digitized and processed using a 1/N-times as fast clock rate of 125 Megahertz (MHz). Thus, each bit can be processed for 8 nanoseconds, which is achievable with currently available technology.

[0008] As shown in FIG. 1, the energy of the received signal is increased by a preamplifier 115 before being sampled by a series of N track and hold circuits 120-1 through 120-N that are each triggered by a respective trigger clock, Φ_1 through Φ_N, that is 1/N-times as fast as the incoming clock rate. The incoming clock, clk, associated with the received data, and the various 1/N-times slower clocks, Φ_1 through Φ_N, are shown in FIG. 2. In this manner, the received data can be processed in parallel at a rate that is 1/N-times as fast as the incoming clock rate. The parallel analog samples are then converted to a digital signal by N analog-to-digital converters 130-1 through 130-N before digital signal processing (DSP) techniques are applied by an adaptive digital signal processor 140 in order to perform data detection, discussed below.

[0009] FIG. 3 illustrates one suitable implementation of the receiver 100 in accordance with the present invention. As shown in FIG. 3, the analog data from the output of the preamplifier 115 (FIG. 1) is applied to N analog-to-digital converters 320-1 through 320-N that are each triggered by a respective trigger clock, Φ_1 through Φ_N, that is 1/N-times as fast as the incoming clock rate. A digital phase locked loop (DPLL) 325 performs clock recovery of the incoming clock signal, clk, associated with the received data, and generates the various 1/N-times faster clocks, Φ_1 through Φ_N. In this manner, the received data is processed in parallel at a rate that is 1/N-times as fast as the incoming clock rate. The digital outputs of the analog-to-digital converters 320-1 through 320-N are stored in N registers 330-1 through 330-N that are all triggered by the same 1/N-times as fast digital clock to resynchronize the parallel branches.

[0010] Since each of the analog-to-digital converters 320-1 through 320-N and corresponding track and hold amplifiers 120-1 through 120-N have a unique offset and gain error, the receiver 100 optionally includes error estimation circuits 340-1 through 340-N, gain control circuits 350-1 through 350-N and offset cancellation circuits 360-1 through 360-N for each of the N parallel branches. Although the error estimation circuit 340-k, gain control circuits 350-k and offset cancellation circuits 360-k are only shown in detail in FIG. 3 for the k-th branch of the receiver 100, corresponding error estimation circuits 340-1 through 340-N, gain control circuits 350-1 through 350-N and offset cancellation circuits 360-1 through 360-N would be included in each of the N parallel branches. A reference signal is applied, and the error estimation circuits 340-1 through 340-N measure the error and generate an error signal, e_N. The error signal is generated by comparing the detected value, X, to a two level quantized value produced by a quantizer 370-1 through 370-N. In one embodiment, the quantizer 370-1 through 370-N receives the value X, and generates an applied reference signal indicating the sign of X (having a value equal to positive or negative 1).

[0011] Generally, if the applied reference signal is a binary "1," and a value of .9 is measured, the error signal, e_N, is 1. The error signal, e_N, is used to update the gain control circuits 350-1 through 350-N and offset cancellation circuits 360-1 through 360-N. As shown in FIG. 3, for the *k*-th parallel branch, the raw output of the analog-to-digital converter 320-k is D_k, and the gain correction circuit 350-k produces a signal A_k, that is gain error free. The corrected and calibrated digital data is referred to as X_k. Each of the individual gain and offset errors are corrected since the incoming symbol on each path is random and cyclostationary (a random variable that periodically has the same statistical properties).

[0012] Thereafter, the digital data, X_k, is operated on by an adaptive digital signal processor 370 that performs channel equalization and data detection to produce the output symbols or bits, b_1 though b_n. As discussed below in conjunction

with FIGS. 4 through 6, the adaptive digital signal processor 370 may be embodied, for example, as an adaptive channel equalizer 500 or a maximum likelihood sequence estimator (MLSE) 650, such as a Viterbi detector.

[0013] FIG. 4 illustrates one suitable implementation of a receiver 100 in accordance with the present invention. As shown in FIG. 4, the receiver 100 includes an analog whitening matched filter (WMF) 410 that preprocesses the analog signal prior to digitization by an analog-to-digital (A/D) converter 420. The digitized data is then processed by an adaptive channel equalizer 500, discussed further below in conjunction with FIG. 5, that produces the output symbols or bits, b_1 though b_n.

[0014] The feedback loop includes a channel estimator 440 that determines appropriate tap weight values to perform clock recovery. In the illustrative implementation, the channel estimator 440 uses the decided symbols from the adaptive channel equalizer 500 to perform blind or decision-directed tap adaptation. The channel estimator 440 is discussed further below in a section entitled PARALLEL IMPLEMENTATION OF A CHANNEL EQUALIZER. The tap weights, h_k, determined by the channel estimator 440 are applied in the clock recovery loop by a phase detector 450 and a low pass filter 460 to select a clock phase and generate the 1/N clocks. Each time the tap weights, h_k, are adjusted, a new clock phase is selected in the clock recovery loop.

[0015] FIG. 5 illustrates the adaptive channel equalizer 500 of FIG. 4. As shown in FIG. 5, the adaptive channel equalizer 500 includes an adaptive feed forward equalizer (FFE) 510 in parallel form, and a slicer 520 that quantizes the digital data. An implementation of the adaptive feed forward equalizer (FFE) 510 is discussed further below in a section entitled PARALLEL IMPLEMENTATION OF A CHANNEL EQUALIZER. An error signal, e_k, is generated in the feedback loop by a summer 530 that adapt the taps of the adaptive feed forward equalizer (FFE) 510. It is noted that the performance of the adaptive channel equalizer 500 can be enhanced using a decision feedback equalizer (DFE) (not shown). For a detailed discussion of parallel decision feedback equalizers (DFEs), see Kalavai J. Raghunath and Keshab Parhi, "Parallel Adaptive Decision Feedback Equalizers," IEEE Trans. on Signal Processing, Vol. 41, No. 5 (May 1993), incorporated by reference herein.

[0016] FIG. 6 illustrates an alternate implementation of a receiver 100 in accordance with the present invention. As shown in FIG. 6, the receiver 100 includes an analog whitening matched filter (WMF) 610 that preprocesses the analog signal prior to digitization by an analog-to-digital (A/D) converter 620. The digitized data is then processed by a maximum likelihood sequence estimator (MLSE) 650, such as a Viterbi detector, that performs data detection without equalization to produce the output symbols or bits, b_1 though b_n. Maximum likelihood sequence estimators (MLSE) 650 consider a number of possible sequences and determines which sequence was actually received, in a known manner. For a more detailed discussion of a Viterbi implementation of a maximum likelihood sequence estimator (MLSE), see Gerhard Fettweis and Heinrich Meyr, "High-Speed Parallel Viterbi Decoding Algorithm and VLSI-Architecture," IEEE Communication Magazine (May 1991), incorporated by reference herein.

[0017] The feedback loop includes a channel estimator 640 that determines appropriate tap weight values to perform maximum likelihood sequence estimation. In the illustrative implementation, the channel estimator 640 uses the decided symbols from the maximum likelihood sequence estimator (MLSE) 630 to perform blind or decision-directed tap adaptation. The channel estimator 640 is discussed further below in a section entitled PARALLEL IMPLEMENTATION OF A CHANNEL EQUALIZER. The tap weights, h_k, determined by the channel estimator 640 are applied in the clock recovery loop by a phase detector 650 and a low pass filter 660 to select a clock phase and generate the 1/N times as fast clocks. Each time the tap weights, h_k, are adjusted, a new clock phase is selected in the clock recovery loop, in a known manner.

Parallel Implementation Of A Channel Equalizer

[0018] As previously indicated, the channel estimators 440 and 640, as well as the adaptive feed forward equalizer (FFE) 510, require parallel implementations of a channel equalizer 700. FIG. 7 illustrates a schematic block diagram of a parallel channel equalizer. Let X represent the input of the channel equalizer 700 and Y the output, and (X_0, X_1, ... X_N) and (Y_0, Y_1, ... Y_N) the parallel representation of X and Y, respectively, where each of the X_k or Y_k values are clocked 1/N-times as fast as X and Y.

[0019] Representing all signals and filter transfer functions with their z transforms:

$$X(z) = X_0(z) + z^{-1}X_1(z) + \ldots + z^{-N+1}X_{N-1}(z) \qquad \text{Eq. (1)}$$

$$H(z) = H_0(z) + z^{-1}H_1(z) + \ldots + z^{-N+1}H_{N-1}(z) \qquad \text{Eq. (2)}$$

where H_j and X_j are given by:

$$H_j(z) = \begin{cases} \sum_{k=0}^{m-1-j} h_{kN+j} z^k & \text{if } m-1 \geq j \\ 0 & \text{if } m-1 < j \end{cases} \quad Eq.(3)$$

and m is the number of taps for the equalizer. Xj(Z) is the subsample at phase j of the input signal X, as shown in FIG. 7. The output Y(z) is given by:

$$Y(z) = H(z)\, X(z) \quad Eq.(4)$$

[0020] For a parallel implementation of the filter H, there is a matrix [A], such that:

$$\begin{pmatrix} Y_0 \\ Y_1 \\ \vdots \\ Y_{N-1} \end{pmatrix} = [A] \begin{pmatrix} X_0 \\ X_1 \\ \vdots \\ X_{N-1} \end{pmatrix} \quad Eq.(5)$$

[0021] It can be shown that:

$$\begin{pmatrix} Y_0 \\ Y_1 \\ Y_2 \\ \vdots \\ Y_{N-1} \end{pmatrix} = \begin{pmatrix} H_0 & z^{-1}H_{N-1} & z^{-1}H_{N-2} & \cdots & z^{-1}H_1 \\ H_1 & H_0 & z^{-1}H_{N-1} & \cdots & z^{-1}H_2 \\ H_2 & H_1 & H_0 & \cdots & z^{-1}H_3 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ H_{N-1} & H_{N-2} & H_{N-3} & \cdots & H_0 \end{pmatrix} \begin{pmatrix} X_0 \\ X_1 \\ X_2 \\ \vdots \\ X_{N-1} \end{pmatrix} \quad Eq.(6)$$

[0022] FIG. 8 illustrates a parallel finite impulse response (FIR) filter 800 that implements Equation 6.

Claims

1. A method for receiving a signal from a dispersible channel, said signal having an incoming clock rate, said method comprising the steps of:

   equalizing said channel using a plurality of parallel paths, each of said paths having a clock rate slower than said incoming clock rate; and
   detecting said signal using a digital signal processor (DSP) that processes said signal using said parallel paths.

2. The method according to claim 1, further comprising the step of sampling said signal on each of said plurality of parallel paths.

3. The method according to claim 1, further comprising the step of digitizing said signal on each of said plurality of parallel paths.

4. The method according to claim 2, wherein said sampling is performed using interleaved analog-to-digital converters.

5. The method according to any of the preceding claims, wherein said equalizing step is performed using N parallel paths, each triggered by a clock that is 1/N-times as fast as said incoming clock rate.

6. The method according to any of the preceding claims, wherein said equalizing and detecting steps are performed using an adaptive channel equalizer.

7. The method according to claim 6, wherein said adapative channel equalizer includes an adaptive feed forward equalizer (FFE).

8. The method according to claim 6, wherein the performance of said adaptive channel equalizer is improved using a decision feedback equalizer (DFE).

9. The method according to any of claims 1 to 5, wherein said detecting step is performed using a maximum likelihood sequence estimator.

10. The method according to claim 9, wherein said maximum likelihood sequence estimator is implemented as a Viterbi detector.

11. A receiver adapted to receive a signal from a channel, said signal having an incoming clock rate, said receiver comprising means for carrying out each step of a method as claimed in any of the preceding claims.

12. A method for calibrating an interleaved analog-to-digital converter to produce a calibrated output of said interleaved analog-to-digital converter, said method comprising the steps of:

generating an error signal for each path of said interleaved analog-to-digital converter by comparing said calibrated output with a quantized version of said calibrated output; and
adjusting a gain control circuit as a function of said error signal.

13. A method for calibrating an interleaved analog-to-digital converter to produce a calibrated output of said interleaved analog-to-digital converter, said method comprising the steps of:

generating an error signal for each path of said interleaved analog-to-digital converter by comparing said calibrated output with a quantized version of said calibrated output; and
adjusting an offset correction circuit as a function of said error signal.

14. The method according to claim 12 or claim 13, wherein said quantizer provides a two level signal indicating whether said calibrated output is higher or lower than an expected value.

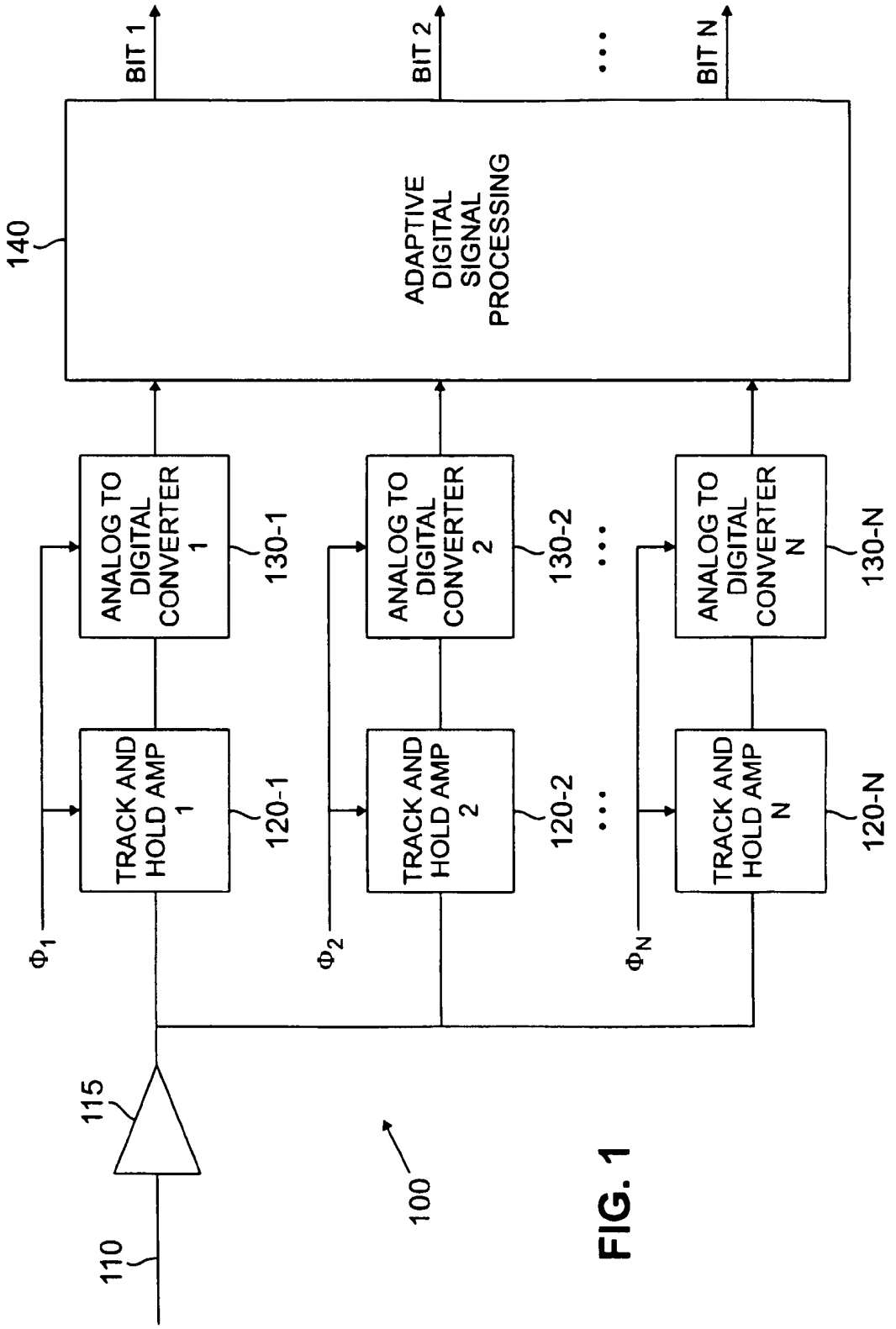
BIT 1
BIT 2
BIT N
140
ADAPTIVE DIGITAL SIGNAL PROCESSING
ANALOG TO DIGITAL CONVERTER 1
130-1
ANALOG TO DIGITAL CONVERTER 2
130-2
ANALOG TO DIGITAL CONVERTER N
130-N
TRACK AND HOLD AMP 1
120-1
TRACK AND HOLD AMP 2
120-2
TRACK AND HOLD AMP N
120-N
Φ1
Φ2
ΦN
115
110
100

FIG. 1

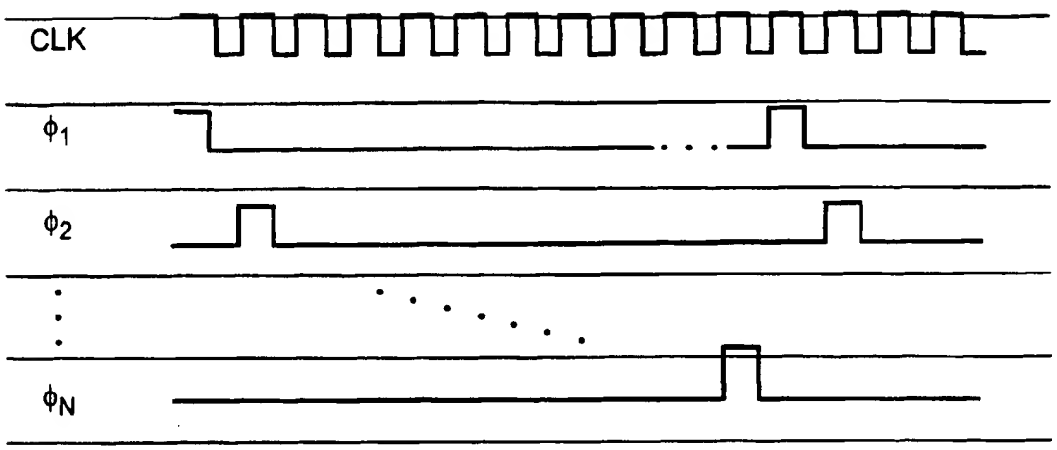
CLK
ϕ_1
ϕ_2
ϕ_N

FIG. 2

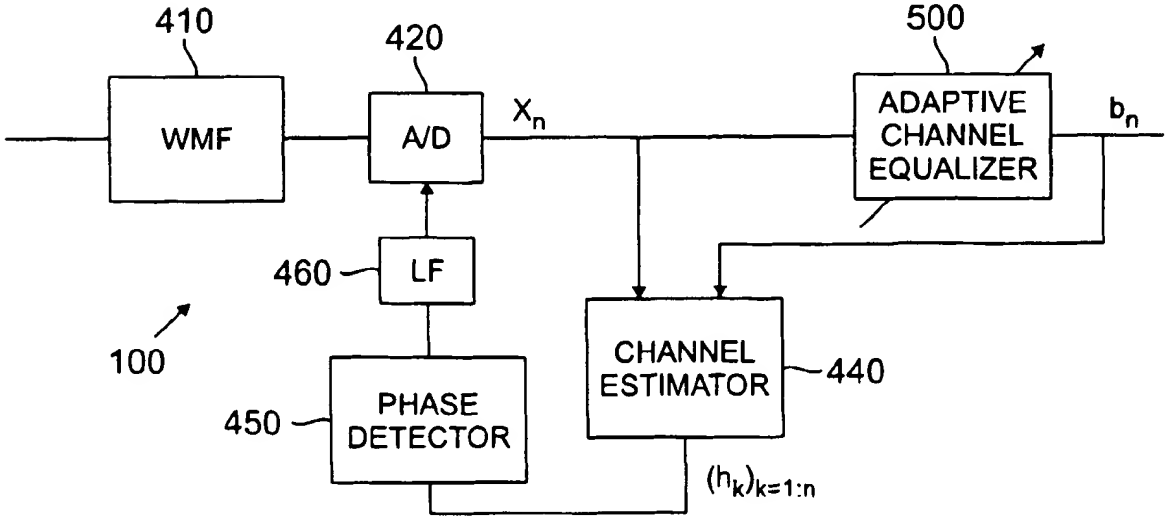
410
420
500
WMF
A/D
X_n
ADAPTIVE CHANNEL EQUALIZER
b_n
460
LF
100
CHANNEL ESTIMATOR
440
450
PHASE DETECTOR
$(h_k)_{k=1:n}$

FIG. 4

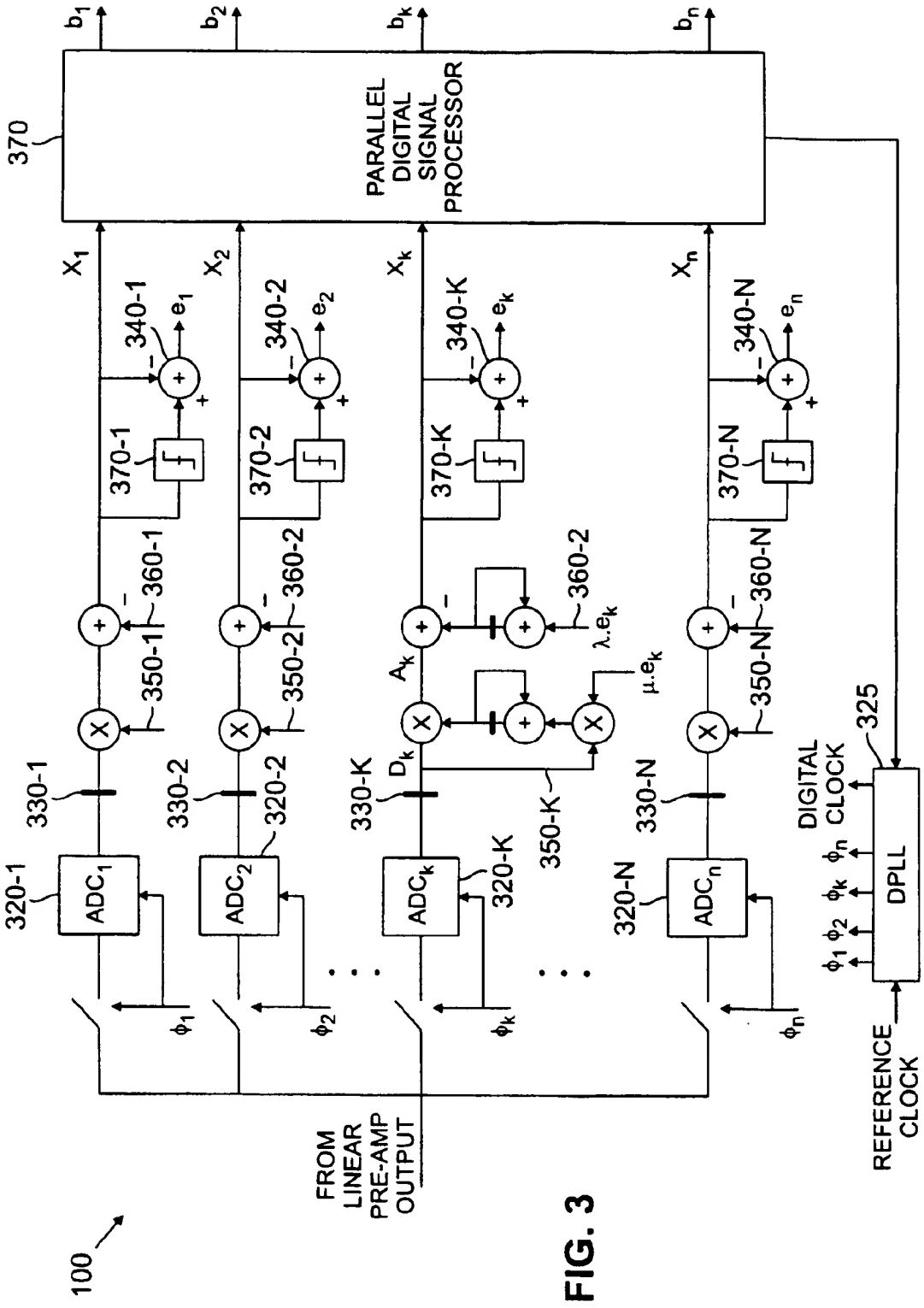
100
370
PARALLEL DIGITAL SIGNAL PROCESSOR
b_1
b_2
b_k
b_n
X_1
X_2
X_k
X_n
340-1
340-2
340-K
340-N
e_1
e_2
e_k
e_n
370-1
370-2
370-K
370-N
360-1
360-2
360-K
360-N
350-1
350-2
350-K
350-N
330-1
330-2
330-K
330-N
320-1
320-2
320-K
320-N
ADC_1
ADC_2
ADC_k
ADC_n
A_k
D_k
$\lambda.e_k$
$\mu.e_k$
ϕ_1
ϕ_2
ϕ_k
ϕ_n
DIGITAL CLOCK
325
DPLL
REFERENCE CLOCK
FROM LINEAR PRE-AMP OUTPUT

FIG. 3

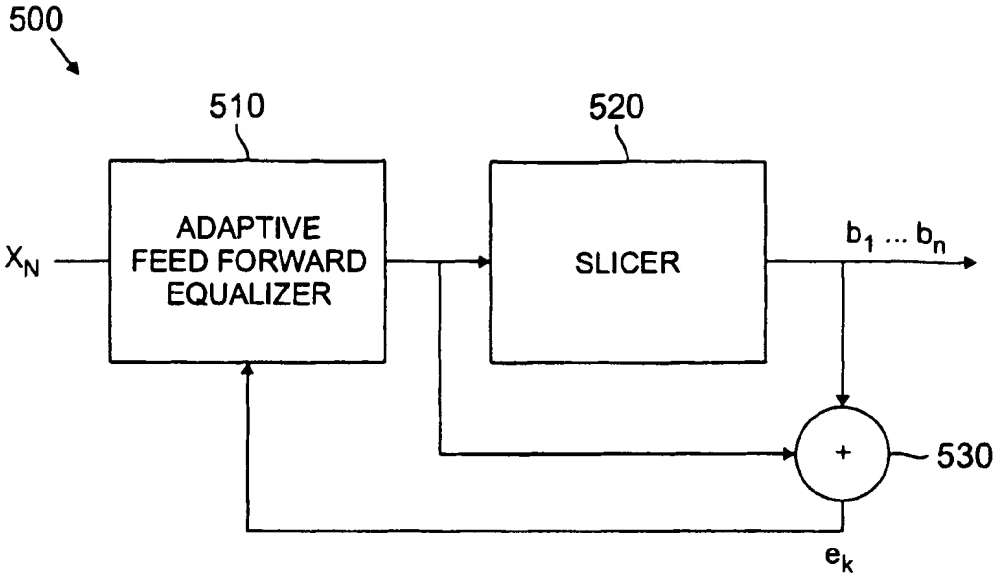
500
510
520
ADAPTIVE FEED FORWARD EQUALIZER
SLICER
X_N
$b_1 \ldots b_n$
+
530
e_k

FIG. 5

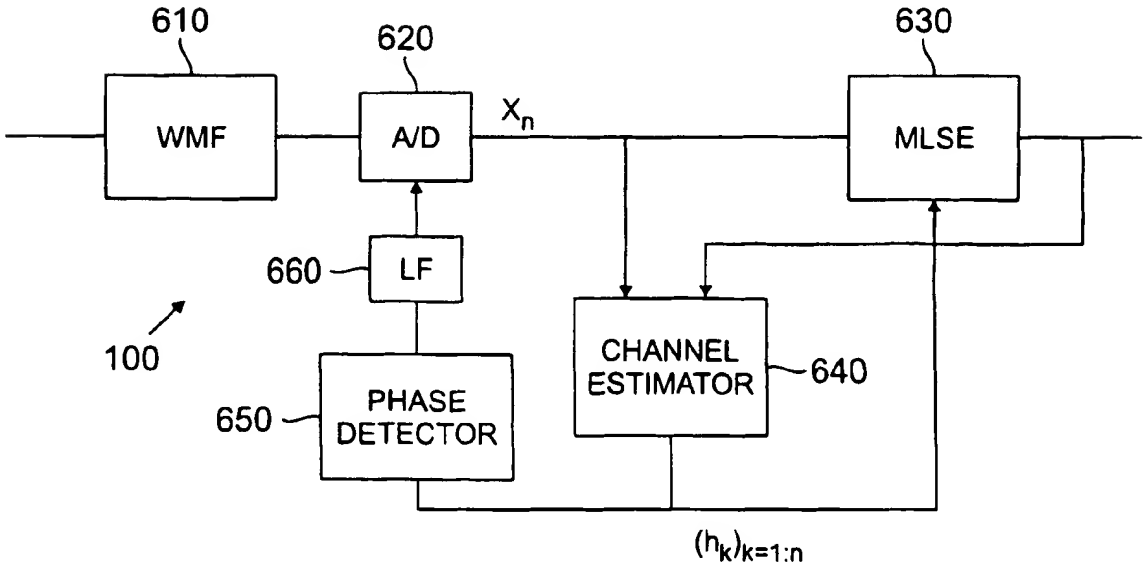
610
620
630
WMF
A/D
X_n
MLSE
660
LF
100
CHANNEL ESTIMATOR
640
650
PHASE DETECTOR
$(h_k)_{k=1:n}$

FIG. 6

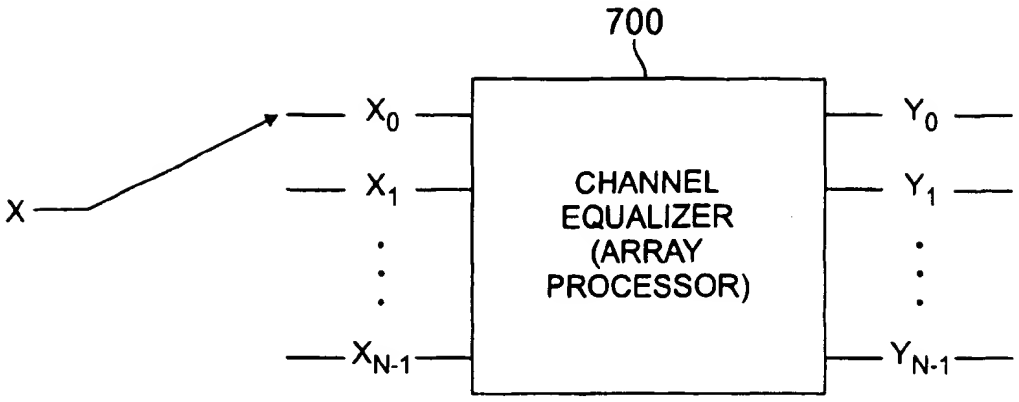
700
X
X_0
X_1
X_{N-1}
CHANNEL EQUALIZER (ARRAY PROCESSOR)
Y_0
Y_1
Y_{N-1}

FIG. 7

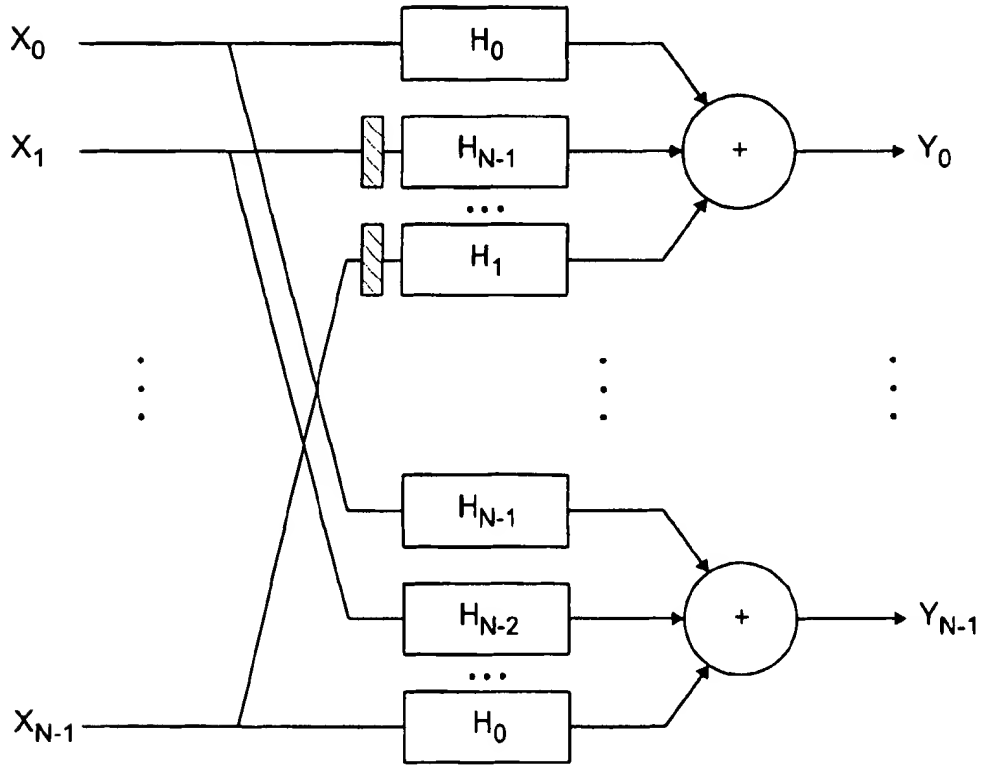
X_0
X_1
X_{N-1}
H_0
H_{N-1}
H_1
H_{N-1}
H_{N-2}
H_0
+
+
Y_0
Y_{N-1}

FIG. 8

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 006 697 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
02.01.2004 Bulletin 2004/01

(43) Date of publication A2:
07.06.2000 Bulletin 2000/23

(21) Application number: **99309305.3**

(22) Date of filing: **23.11.1999**

(51) Int Cl.[7]: **H04L 25/03**, H04L 25/06

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **02.12.1998 US 203969**

(71) Applicant: **LUCENT TECHNOLOGIES INC.**
Murray Hill, New Jersey 07974-0636 (US)

(72) Inventors:
- **Azadet, Kameran**
  Middletown, New Jersey 07748 (US)
- **Yu, Meng-Lin My**
  Morganville, New Jersey 07751 (US)

(74) Representative: **Williams, David John et al**
Page White & Farrer,
54 Doughty Street
London WC1N 2LS (GB)

(54) Parellel signal processing for equalisation on fibre channels

(57) A method and apparatus are disclosed for reducing dispersion problems in data signals received over a channel, such as a fiber channel. A receiver processes the received data on parallel branches at a rate that is slower than the original clock rate. Channel equalization techniques can thus be applied to fiber channels despite the very high clock rates of the received signal. The clock rate of the received signal is reduced by an arbitrary factor N for sampling and digitizing the analog signal at the output of the fiber channel. The parallel analog samples are digitized before digital signal processing (DSP) techniques are applied by an adaptive digital signal processor to perform data detection. The adaptive digital signal processor may be embodied, for example, as an adaptive channel equalizer that utilizes an adaptive feed forward equalizer (FFE), or as a maximum likelihood sequence estimator (MLSE), such as a Viterbi detector.

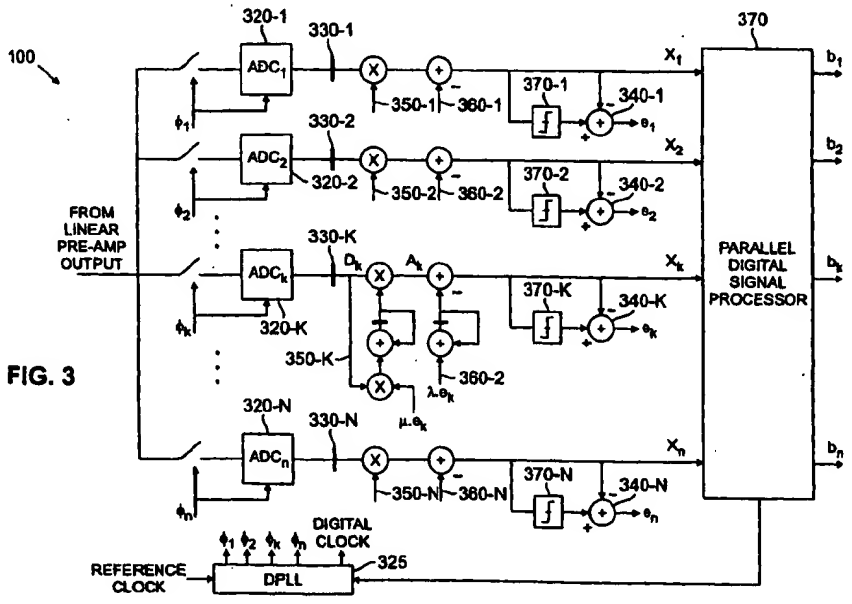

FIG. 3

EP 1 006 697 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 9305

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X Y	WO 98 39871 A (LEVEL ONE COMMUNICATIONS INC) 11 September 1998 (1998-09-11) * abstract * * page 2, line 1 - line 30 * * page 5, line 35 - page 6, line 10 * * page 8, line 25 - page 11, line 20 * ---	1-4,6-8, 11-14 5	H04L25/03 H04L25/06
Y A	DE 43 32 735 A (BOSCH GMBH ROBERT) 30 March 1995 (1995-03-30) * column 1, line 50 - line 60 * * column 2, line 60 - column 3, line 20 * * column 3, line 30 - line 45 * * column 4, line 60 - column 5, line 10 * * column 6, line 20 - line 55 * ---	5 1-4,11	
X Y	US 5 648 988 A (IWAMATSU TAKANORI ET AL) 15 July 1997 (1997-07-15) * column 1, line 40 - line 55 * * column 2, line 10 - line 20 * * column 2, line 40 - column 3, line 20 * ---	1-4,6-8, 11 5	
Y A	PARIS B-P ET AL: "Modulation classification in unknown dispersive environments" ACOUSTICS, SPEECH, AND SIGNAL PROCESSING, 1997. ICASSP-97., 1997 IEEE INTERNATIONAL CONFERENCE ON MUNICH, GERMANY 21-24 APRIL 1997, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 21 April 1997 (1997-04-21), pages 3853-3856, XP010226642 ISBN: 0-8186-7919-0 * page 3854, right-hand column, paragraph 2 - page 3855, left-hand column, paragraph 1 * --- -/--	5 1,2,6,8	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H04L H03M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 October 2003	Litton, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 9305

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	RAGHUNATH K J ET AL: "Parallel adaptive decision feedback equalizers" DIGITAL SIGNAL PROCESSING 2, ESTIMATION, VLSI. SAN FRANCISCO, MAR. 23 - 26, 1992, PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON ACOUSTICS, SPEECH AND SIGNAL PROCESSING (ICASSP), NEW YORK, IEEE, US, vol. 5 CONF. 17, 23 March 1992 (1992-03-23), pages 353-356, XP010059092 ISBN: 0-7803-0532-9 * abstract * * page 353, right-hand column, paragraph 3 * * page 354, left-hand column, paragraph 4 - right-hand column, paragraph 2 *	1-4,6,8	
X	EP 0 379 375 A (NIPPON ELECTRIC CO) 25 July 1990 (1990-07-25) * abstract * * column 1, line 1 - line 35 * * column 2, line 1 - column 3, line 20 *	1-4,6	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
X	WO 98 45955 A (WEBSTER STEPHEN I ;GENNUM CORP (CA)) 15 October 1998 (1998-10-15) * page 6, line 1 - line 10 * * figure 4 *	12-14	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 October 2003	Litton, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 9305

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	PAPADIAS C B ; SLOCK D T M: "Fractionally spaced equalization of linear polyphase channels and related blind techniques based on multichannel linear prediction" IEEE TRANS. SIGNAL PROCESS. (USA), IEEE TRANSACTIONS ON SIGNAL PROCESSING, MARCH 1999, IEEE, USA, vol. 47, no. 3, - 1 March 1999 (1999-03-01) pages 641-654, XP002249654 * page 642, left-hand column, paragraph 4 - right-hand column, paragraph 3 * * page 644, left-hand column, paragraph 2 - right-hand column, paragraph 2 * * page 650, right-hand column, paragraph 3 - page 651, left-hand column, paragraph 1 * ---	1-8,11	
A	WO 96 35284 A (BOERJESSON PER OLA ;OEDLING PER M (SE); ERIKSSON B HAAKAN (SE)) 7 November 1996 (1996-11-07) * page 1, line 25 - page 2, line 2 * * page 4, line 15 - line 35 * * page 5, line 30 - page 6, line 2 * -----	1-4,9	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 October 2003	Litton, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 99 30 9305

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 99 30 9305

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-11

   A method of equalising high bitrate data using a polyphase parallel approach, whereby each of the N parallel paths equalise data at 1/Nth the original bitrate.

2. Claims: 12-14

   A method of determining and accounting for discrepencies, such as gain errors and offset errors, in an A/D converter.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 30 9305

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

17-10-2003

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
WO 9839871	A	11-09-1998	US	6167082 A	26-12-2000
			AU	6685098 A	22-09-1998
			EP	0965207 A2	22-12-1999
			WO	9839871 A2	11-09-1998
DE 4332735	A	30-03-1995	DE	4332735 A1	30-03-1995
			FR	2710473 A1	31-03-1995
			GB	2282303 A ,B	29-03-1995
			JP	3294017 B2	17-06-2002
			JP	7170191 A	04-07-1995
US 5648988	A	15-07-1997	WO	9406233 A1	17-03-1994
			JP	7500959 T	26-01-1995
			US	5495501 A	27-02-1996
EP 0379375	A	25-07-1990	JP	1880360 C	21-10-1994
			JP	2190033 A	26-07-1990
			JP	6005822 B	19-01-1994
			AU	617076 B2	14-11-1991
			AU	4856990 A	26-07-1990
			CA	2007922 A1	19-07-1990
			DE	69013524 D1	01-12-1994
			DE	69013524 T2	08-06-1995
			EP	0379375 A2	25-07-1990
			US	5005185 A	02-04-1991
WO 9845955	A	15-10-1998	CA	2201834 A1	04-10-1998
			US	6304615 B1	16-10-2001
			AU	6817998 A	30-10-1998
			WO	9845955 A2	15-10-1998
			EP	0972347 A2	19-01-2000
			JP	2001519107 T	16-10-2001
			US	2002034221 A1	21-03-2002
WO 9635284	A	07-11-1996	WO	9635284 A1	07-11-1996

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82